

CMD65R580/CMU65R580

650V N-Channel Super Junction Power MOSFET

General Description

The 65R580 series use advanced MOSFET technology to provide low $R_{DS(ON)}$ low gate charge, fast switching and excellent avalanche characteristics. This device is suitable for active power factor correction and switching mode power supply applications.

Features

- Multi-layer Epitaxial Chip Technology
- Low On-Resistance
- 100% Avalanche Tested
- RoHS Compliant

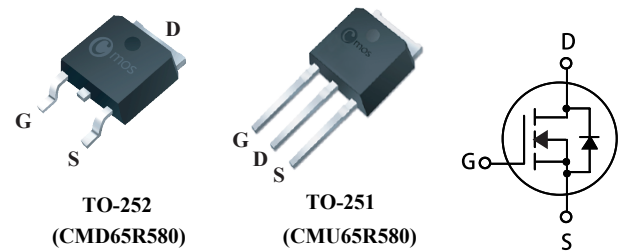
Product Summary

BVDSS	$R_{DS(ON)}$	ID
650V	0.62 Ω	8A

Applications

- Power Supply
- PFC
- Switching Applications

TO-252/251 Pin Configuration



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	650	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	8	A
	- Continuous ($T_C = 100^\circ\text{C}$)	5	A
I_{DM}	Drain Current - Pulsed	24	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ¹	170	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	45	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Value	Units
$R_{\theta C}$	Thermal Resistance, Junction-to-Case Max.	2.75	$^\circ\text{C/W}$
$R_{\theta A}$	Thermal Resistance, Junction-to-Ambient Max	62.5	$^\circ\text{C/W}$

Electrical Characteristic

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	--	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.5\text{A}$	--	0.55	0.62	Ω
R_G	Gate resistance	$f = 1\text{MHz}$, open drain	--	27	--	Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	--	500	--	pF
C_{oss}	Output Capacitance		--	430	--	pF
C_{rss}	Reverse Transfer Capacitance		--	25	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 300\text{ V}, V_{GS} = 10\text{ V}$ $I_D = 8\text{ A}$ $R_G = 25\Omega$	--	15	--	ns
t_r	Turn-On Rise Time		--	35	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	76	--	ns
t_f	Turn-Off Fall Time		--	33	--	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}$ $I_D = 8\text{ A}$ $V_{GS} = 10\text{ V}$	--	17.5	--	nC
Q_{gs}	Gate-Source Charge		--	5	--	nC
Q_{gd}	Gate-Drain Charge		--	7	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	24	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 5A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	I _F = 8 A , V _{DD} = 100V dI / dt = 100 A/us	--	260	--	ns
Q _{rr}	Reverse Recovery Charge		--	2	--	μC

Note :

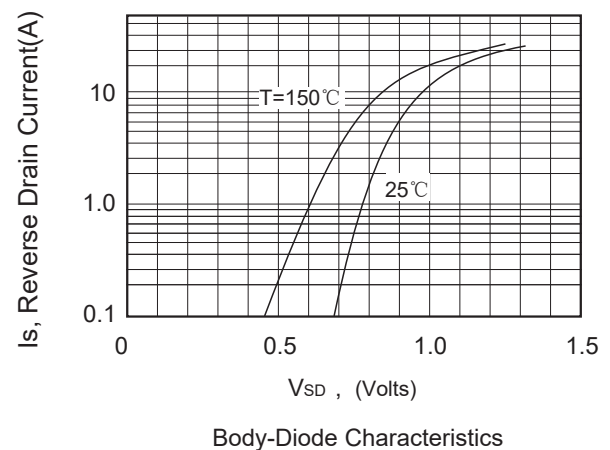
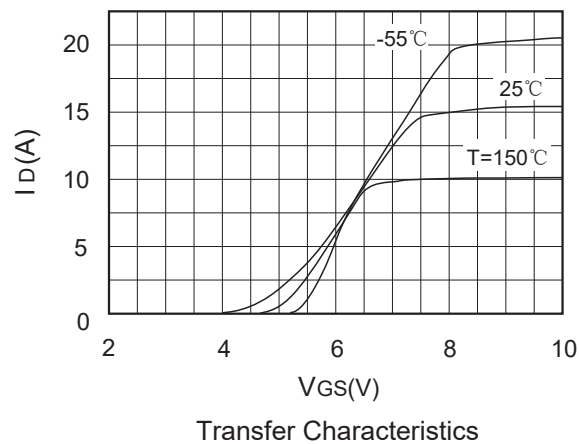
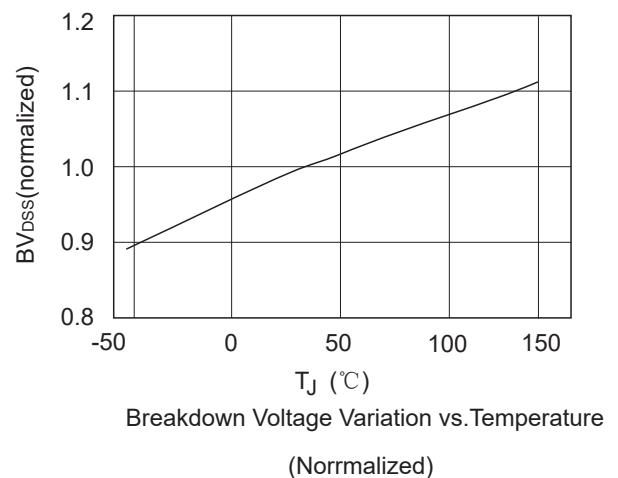
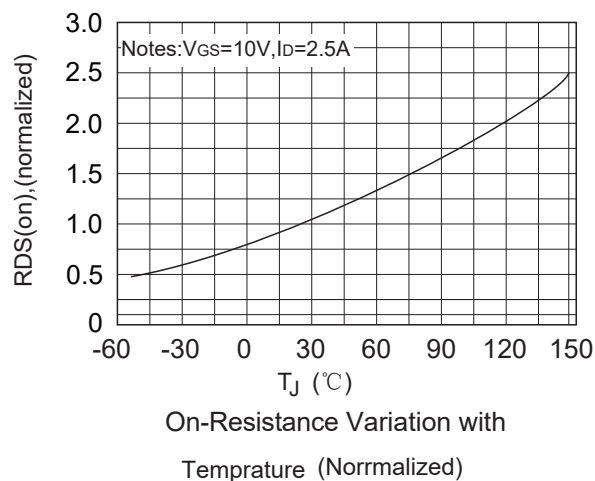
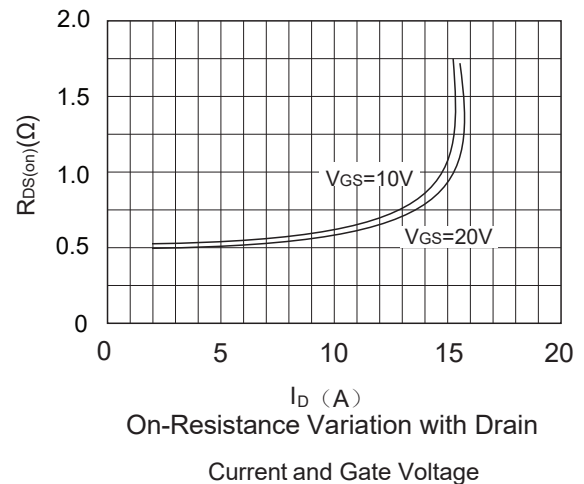
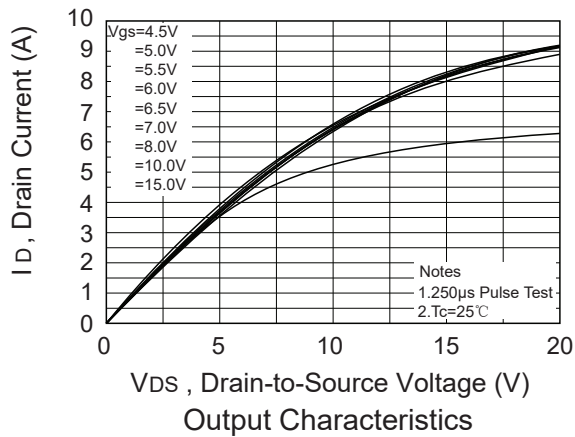
1. The EAS data shows Max. rating . The test condition is $V_{DD} = 80\text{ V}, V_{GS} = 10\text{ V}, L = 20\text{ mH}, I_{AS} = 3.4\text{ A}$.

This product has been designed and qualified for the consumer market.

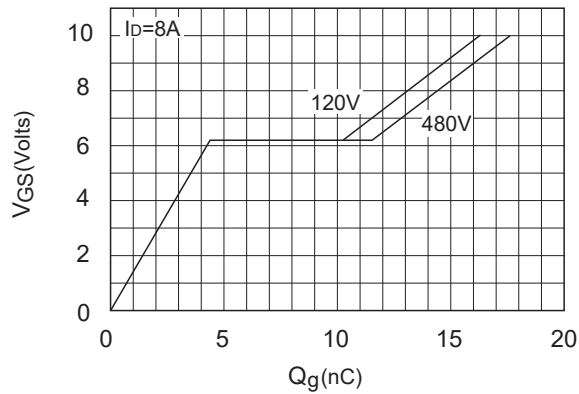
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Cmos reserves the right to improve product design, functions and reliability without notice.

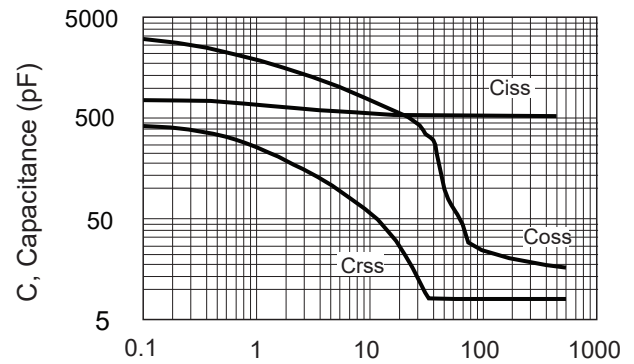
Typical Characteristics



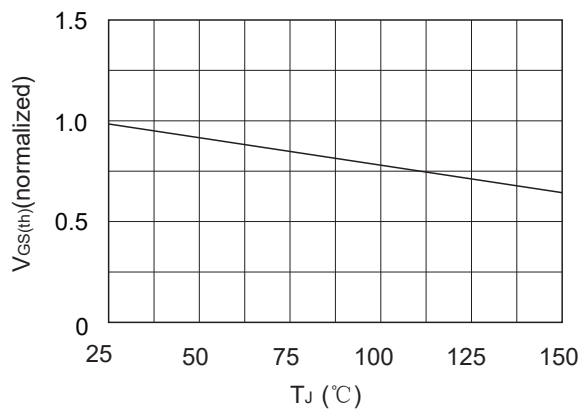
Typical Characteristics



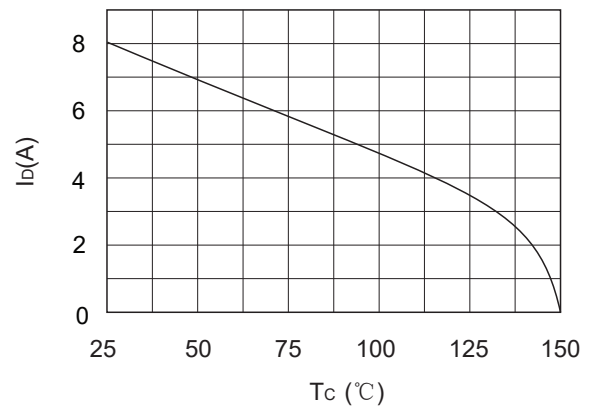
Gate-Charge Characteristics



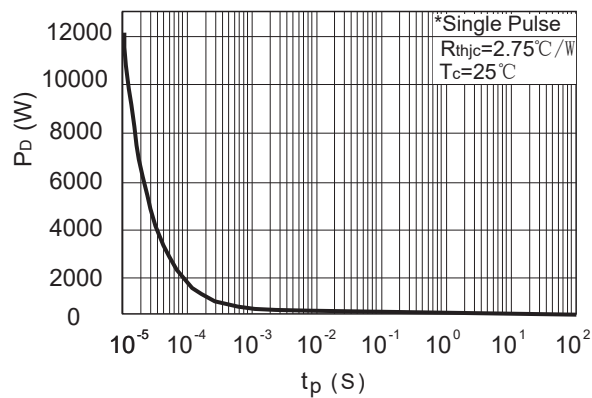
Capacitance Characteristics



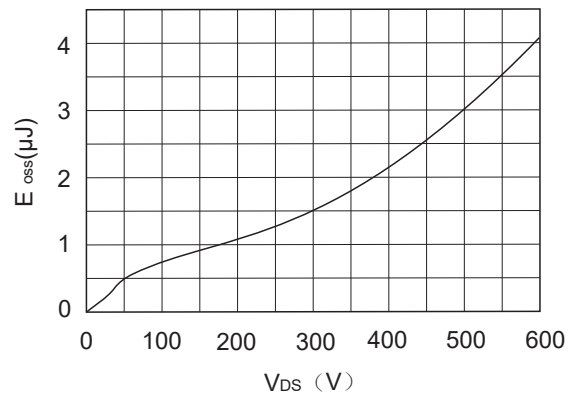
$V_{GS(th)}$ Variation with Temperature(Nomalized)



Maximum Drain Current vs Case Temperature

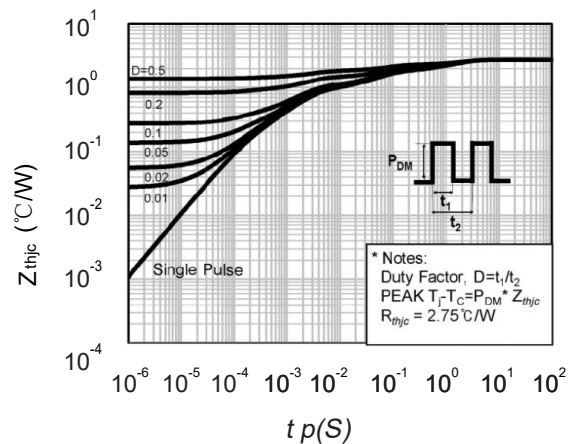


Single Pulse Maximum Power Dissipation

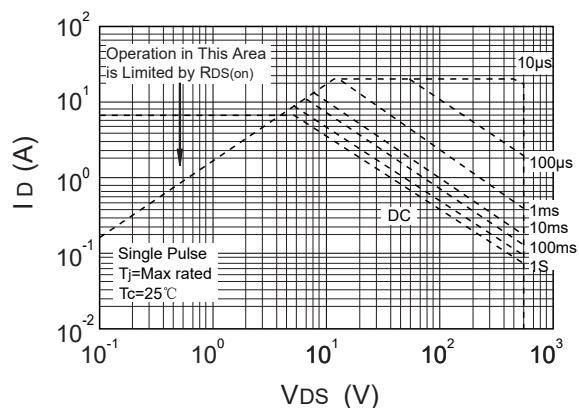


Output Capacitance Stored Energy

Typical Characteristics



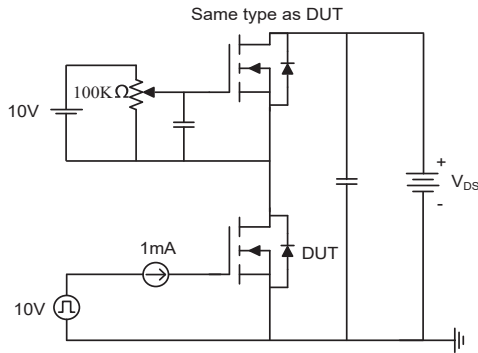
Transient Thermal Response Curve



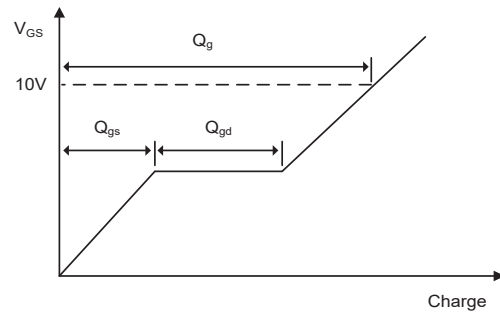
Maximum Safe Operating Area

Test Circuit

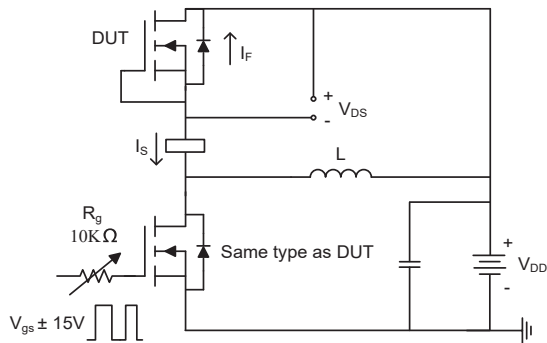
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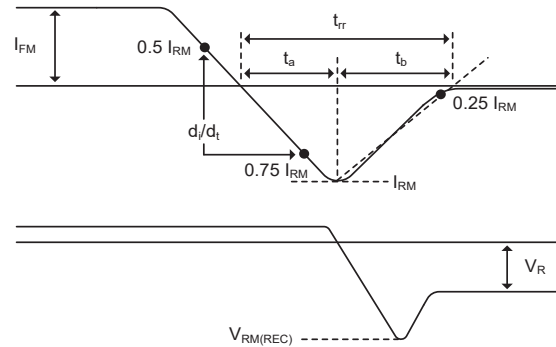
Gate charge measurement circuit



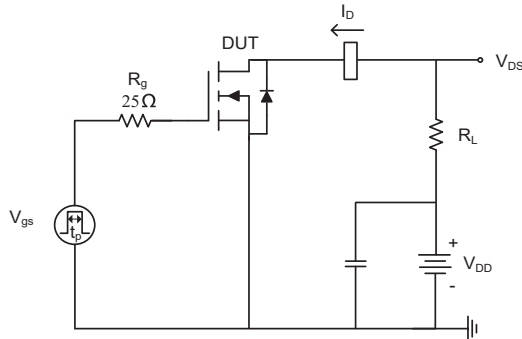
Gate charge waveform



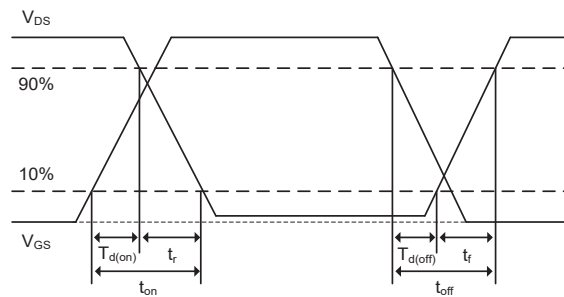
Diode reverse recovery test circuit



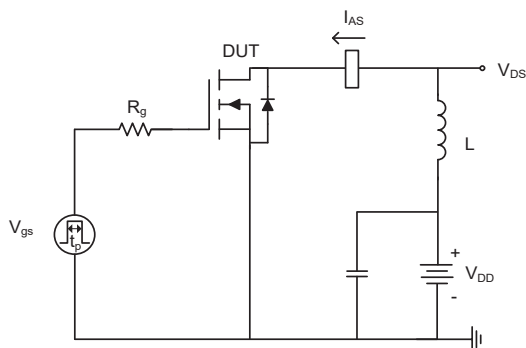
Diode reverse recovery test waveform



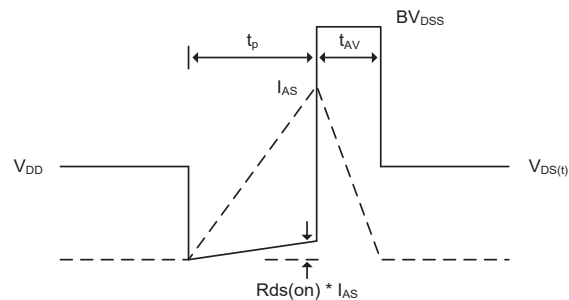
Switching time test circuit for resistive load



Switching time waveform



Unclamped inductive load test circuit



Unclamped inductive waveform